Remarks

Claims 1, 3-16 and 18-20 are in the application. Claims 2 and 17 have been canceled.

The Examiner objects to the drawings, specifically Figure 8, under 37 CFR 1.83(a) and to the description, specifically paragraph [0029]. The Examiner indicates that the aggregator must be shown in Figure 8.

In order to clarify the relationship between Figures 7 and 8, Figure 7 has been amended to label the N grain wide channel **203**. Paragraph [0028] has also been amended accordingly. Figure 8 has been amended to show the aggregated N grain wide channel 203, and its relationship to the MESS egress ports 204, which are also now both separately labeled in Figure 8. As such, Figure 8 now shows the relationship between the grains received on the N grain wide channel 203, as provided by an aggregator such as the aggregator 202 shown in Figure 7. The aggregator 202 need not be shown in Figure 8, which is already shown in Figure 7. Accordingly, it is respectfully submitted that the figures and the drawings now comply with 37 CFR 1.83(a) and that appropriate correction to the specification has been made.

In the outstanding Office Action, the Examiner indicated that claims 6 and 17 would be allowable if rewritten in independent form. Claim 6 has been rewritten as an independent claim including the subject matter of previous claims 1, 4 and 5. As such, claim 6 is allowable as indicated by the Examiner.

Claim 16 has been rewritten to include the subject matter of previous claim 17, which now has been canceled. As such, amended claim 16 is allowable as indicated by the Examiner. Claims 18-20, by virtue of their ultimate of their dependence on amended claim 16 are allowable for the same reasons.

The Examiner also indicated that claim 13 would be allowable if rewritten to overcome the rejection under 35 USC 112 second paragraph, and to include all of the limitations of the base claim and the intervening claims. Claim 13 has been amended to include the subject matter of previous claims 1, 4, 7 and 12. The expression "the interest RAM" has been replaced with "an

interest RAM", thereby overcoming the rejection under 35 USC 112 second paragraph. As such, amended claim 13 is allowable as indicated by the Examiner.

Claim 1 has been amended to specify that the at least one memory egress self selection egress port is for storing a single grain for each channel, and for transmitting stored data grains in a predetermined order. Claim 1 has also been amended to specify that the at least one predetermined criterion on which the data grains are selected from the received data grains based on the ingress port associated with the received data grains and a position of a grain in its respective grain group, both of which are independent of contents of the received data grains. Support for these amendments is found at least at paragraphs [0032], [0034], [0038] and [0039] of the specification as originally filed. The basis of the predetermined criterion is also found in original claim 17, which the examiner indicated is allowable.

Claim 5 has been amended to specify that the finite state machine is for selecting grains from the aggregate for storage in accordance with the grain mask by compacting incoming data grains into data memory at each egress port to remove gaps between the selected grains. Support for these amendments is found at least at paragraphs [0030] and [0040] of the specification as originally filed.

Claim 7 has been amended to specify that the memory at each of the MESS egress ports includes a plurality of RAMS for storing a received grain. Support for this amendment is found at least in Figures 11-13 and associated paragraphs [0034] – [0043] of the specification as originally filed.

The Examiner rejects claims 1-4, 7, 8, 10-12, 14-16 and 18-20 under 35 USC 102(e) as being anticipated by Walrand et al. The applicant respectfully submits that Walrand (US 7,046,665) pertains to a completely different art area than the current application. Its abstract states "In accordance with the invention, a system and method for providing QOS to packets formatted in accordance with one protocol (e.g., IP or Ethernet) carried over networks that are originally designed to be used with another protocol (e.g., ATM, WDM, or TDM)." It further states that "Such a modified switch can identify IP packets, determine if any packets should be dropped, classify the packets with a queue, and schedule the packet of the queue in a manner that provides quality of service". The current application does not deal with packets at all. It deals

with Time-Division-Multiplexed (TDM) data. All data is treated identically and is thus not classified. No data is dropped as a result of the operations of the switch. The inventive elements of Walrand and those of the current application are completely different. Looking at Figure 4 of Walrand, the current invention relates only to element 402, on which Walrand provides no teachings. The claimed invention can improve the cost and size of element 402.

With regard to the rejection of claim 1, Walrand discloses enhancements *surrounding* a TDM switch such that it can handle packet and provide QOS for them. The enhancements are provided *external to the switch itself.* The TDM switch (element 402) is used as a function within the Walrand switch (element 400). No guidance is given on its construction. The only mention of element 402 in Walrand is: "Because the "switching fabric" 402 is the main part of a conventional switch (e.g. ATM or TDM), "switching fabric" 402 will frequently be referred to as a "switch" or "conventional switch".". It is clear from the disclosure, Walrand did not intend any novel improvements on element 402. In contrast, the instant application provides a novel way to build *TDM switches* (such as element 402) that are much smaller and cheaper than prior art approaches.

In Walrand Figure 4, element 408 is a classifier, which examines each packet and places them onto appropriate queues. (Please see Walrand column 7, lines 62-66). As recited in amended claim 1, the device in the current application does not examine the contents of the data stream, but rather *selects grains in accordance with the ingress port associated with the position of the grain and the position of the grain in its respective grain group.* It is, therefore, not possible to perform any classification as envisioned by Walrand. Thus, the current application does not contain functionality related to element 408 of Walrand.

After classification, packets in Walrand are sent to queuing module (element 410), which determines if the packet is to be sent to the switching fabric or discarded to avoid congestion (Please see Walrand col. 6, lines 43-51). The device in the current application does not drop data. Also, element 410 can store multiple packets in each queue. As recited in amended claim 1, the device in the current application *stores only a single grain for each channel in the egress port.* The reason for the difference lies in Walrand being a packet switch (Walrand col. 2, lines 14-49) and the current application being a TDM switch (Walrand col. 1, line 58 – col. 2,

line 9). Thus, the current application does not contain functionality related to element 410 of Walrand.

Walrand provides a detailed description of the scheduling action performed by element 412. It is disclosed that the Walrand switch can select which packet to output based on a diverse set of parameters. In the current application, since the stored data grains are transmitted in a predetermined order, and they are received at fixed intervals, this means they are transmitted at a time determined by the network. Unlike Walrand, the device has no freedom to determine when or on which port, a data grain is output. Please see Walrand column 1, lines 38-58 for a description of the properties of TDM switching. Stream i must be sent at time T(1) + T(2) + … T(i-1). Thus, the current application does not include a scheduler as envisioned by Walrand.

The applicant respectfully submits that the memory egress self selection (MESS) egress port is not the sum of the elements in Walrand. The current application is a novel way of implementing a TDM switching fabric that may be used to improve the size and cost of element 402 in Walrand.

With regard to claim 3, element 408 of Walrand looks into fields within the incoming packets to determine which queue the packet is to be sent. In the current application, an egress port *selects a grain for buffering based on it location within a TDM frame*, as recited in amended claim 1. The decision is based on time/location, not the data value of the grain itself. Thus, there is no relationship to element 408 of Walrand.

With regard to claim 4, please note that in addition to packet type (TCP, or UDP), Walrand makes drop decisions on buffer full levels (col. 6, 51-53) and on the number of packets in the buffer (col. 6, lines 53-55). As recited in amended claim 1, upon which claim 4 depends, *the device in the current application provides exactly one buffer for each grain*. Each grain is associated with a different communications stream. The buffered grain is read out at the next frame. It is impossible for the buffer to be full and impossible to have variable number grains in the buffer of each communications stream. Thus, there is no relationship to element 410 of Walrand.

With regard to claim 7, element 410 of Walrand is located on the ingress single of his packet switch. It stores multiple (varying number) packets. A control module in combination with a scheduling module determines which packet to inject into the switching fabric, at which time. In the current application, data from ingress ports are sent to all egress ports immediately upon arrival. Please see Figure 7 of the current application, i.e. there is no buffering and thus no decision on injection times. At each egress port, there is *a single (exactly one) buffer element for each grain in the TDM frame*. All of the buffers will be occupied at the end of the frame. Each buffer will only be associated with a single incoming grain. The number of grains is fixed. The device in the current application differs from 410 of Walrand by having buffers on the egress side and having a fixed number of grains.

Also with respect to claim 7, the applicant respectfully submits that the scheduler (element 412) in Walrand need not have any Multiplexors. Its job is to determine the time at which each packet is to be sent (col. 5, lines 29-30) into the switch fabric. Any physical switching from queues to egress interfaces (element 406) can be done by the switching fabric.

With regard to claim 20, the scheduler in Walrand determines the order in which packets are read out. It is free to choose the times as long as certain performance criteria are met. In the current application a grain is read out at the time the network desires it to be read out. The device in the current application has no freedom to change the time.

The Examiner also rejects claims 5 and 9 under 35 USC 103(a) as being unpatentable over Walrand in view of Bianchini. With regard to claim 5, the applicant respectfully submits that Bianchini (US 7,031,330) does not provide material teachings related to the current application. In Bianchini, there is a central shared memory (Fig 4, element 42). In the current application, each egress port has its own memory that is not shared. Finite state machines in Bianchini that schedule writing and reading from the shared memory is not needed in the current application. None of the steps shown in Bianchini col. 5 line 57 to col. 6, line 18 are present in the current application. In contrast, as recited in amended claim 5, *the finite state machine in the current application (Fig 12) compacts incoming data grains into the set of data memory at each egress ports such that there are no holes*. The process is akin to building a brick wall one brick at a time, one row at a time. This procedure bears no resemblance to Bianchini col. 5 line 57 to col. 6, line 18.

With regard to claim 9, the applicant respectfully requests guidance on where in Walrand multiplexors are intimated with respect to element 408. Col 5, lines 25-26 describes a logical function of assigning packets to queues. The actual implementation need not involve multiplexors. For example, the packets may be written into a single shared memory, as in Bianchini, and associated to various queues via software pointers. Unless Walrand demonstrates how multiplexors can be used to improve upon TDM switches, it would not be obvious to anyone skilled in the art to take Col 5, lines 25-26 and invent the compaction algorithm as disclosed in the current application.

In view of the amendments and arguments described above, the Applicant respectfully submits that all of the pending claims comply with 35 USC 102(e) and 35 USC 103(a), and withdrawal of those objections is respectfully requested.

The Applicant submits that the present application is now in condition for allowance, and looks forward to receiving a Notice of Allowability. The Examiner is invited to contact the undersigned to discuss any issues that may be need to be addressed to bring this case to allowance.

The Commissioner is hereby authorized to debit $460.00 from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP, representing the fees for a two month extension of time.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

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